14-Bit, 125 MSPS TxDAC® D/A Converter

AD9764

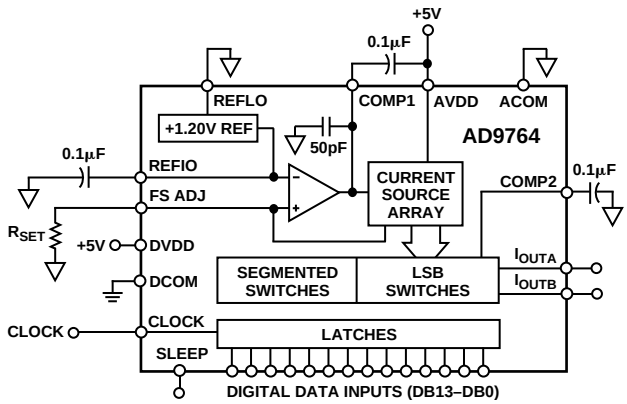
FEATURES

Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
14-Bit Resolution
Excellent SFDR and IMD
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 190 mW @ 5 V to 45 mW @ 3 V
Power-Down Mode: 25 mW @ 5 V
On-Chip 1.20 V Reference
Single +5 V or +3 V Supply Operation
Packages: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS

Communication Transmit Channel:
Basestations
ADSL/HFC Modems
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9764 is the 14-bit resolution member of the TxDAC series of high performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, providing an upward or downward component selection path based on performance, resolution and cost. The AD9764 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9764's flexible single-supply operating range of 2.7 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 45 mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 25 mW.

The AD9764 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3 V and +5 V CMOS logic families.

The AD9764 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9764 can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows the AD9764 full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the AD9764 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9764 is available in 28-lead SOIC and TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9764 is a member of the TxDAC product family that provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost.
2. Manufactured on a CMOS process, the AD9764 uses a proprietary switching technique that enhances dynamic performance beyond that previously attainable by higher power/cost bipolar or BiCMOS devices.
3. On-chip, edge-triggered input CMOS latches readily interface to +3 V and +5 V CMOS logic families. The AD9764 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of 2.7 V to 5.5 V, and a wide full-scale current adjustment span of 2 mA to 20 mA, allows the AD9764 to operate at reduced power levels.
5. The current output(s) of the AD9764 can be easily configured for various single-ended or differential circuit topologies.

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AD9764* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9764 Evaluation Board

DOCUMENTATION

Application Notes

- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-302: Exploit Digital Advantages in an SSB Receiver
- AN-320A: CMOS Multiplying DACs and Op Amps Combine to Build Programmable Gain Amplifier, Part 1
- AN-420: Using the AD9708/AD9760/AD9701/AD9764-EB Evaluation Board
- AN-595: Understanding Pin Compatibility in the TxDAC® Line of High Speed D/A Converters
- AN-912: Driving a Center-Tapped Transformer with a Balanced Current-Output DAC

Data Sheet

- AD9764: 14-Bit, 125 MSPS TxDAC® D/A Converter Data Sheet

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD9764 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9764 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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AD9764–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = +25°C	–4.5	±2.5	+4.5	LSB
T_{MIN} to T_{MAX}	–6.5		+6.5	LSB
Differential Nonlinearity (DNL)				
T_A = +25°C	–2.5	±1.5	+2.5	LSB
T_{MIN} to T_{MAX}	–4.5		+4.5	LSB
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	–2	±1	+2	% of FSR
Gain Error (With Internal Reference)	–7	±1	+7	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth (w/o C_{COMP1})[4]		1.4		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD[5]	2.7	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})		25	30	mA
Digital Supply Current (I_{DVDD})[6]		1.5	4	mA
Supply Current Sleep Mode (I_{AVDD})		5.0	8.5	mA
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		133	170	mW
Power Dissipation[7] (5 V, I_{OUTFS} = 20 mA)		190		mW
Power Dissipation[7] (3 V, I_{OUTFS} = 2 mA)		45		mW
Power Supply Rejection Ratio[8]—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[8]—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

[1]Measured at I_{OUTA}, driving a virtual ground.

[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.

[3]Use an external buffer amplifier to drive any external load.

[4]Reference bandwidth is a function of external cap at COMP1 pin and signal level.

[5]For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.

[6]Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1.0 MHz.

[7]Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at I_{OUTA} and I_{OUTB}, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

[8]±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/$\sqrt{Hz}$
Output Noise (I_{OUTFS} = 2 mA)		30		pA/$\sqrt{Hz}$
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output				
T_A = +25°C	75	82		dBc
T_{MIN} to T_{MAX}	73			dBc
–6 dBFS Output		85		dBc
–12 dBFS Output		77		dBc
–18 dBFS Output		70		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		80		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.51 MHz		77		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz		70		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 20.2 MHz		58		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz; 2 MHz Span				
T_A = +25°C	78	89		dBc
T_{MIN} to T_{MAX}	76			dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		84		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		84		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
T_A = +25°C		–78	–74	dBc
T_{MIN} to T_{MAX}			–72	dBc
f_{CLOCK} = 50 MHz; f_{OUT} = 2.00 MHz		–75		dBc
f_{CLOCK} = 100 MHz; f_{OUT} = 2.00 MHz		–75		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)				
f_{CLOCK} = 20 MSPS; f_{OUT} = 2.00 MHz to 2.99 MHz				
0 dBFS Output		73		dBc
–6 dBFS Output		76		dBc
–12 dBFS Output		73		dBc
–18 dBFS Output		64		dBc

NOTES

[1]Measured single-ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	μA
Logic "0" Current	–10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

Specifications subject to change without notice.

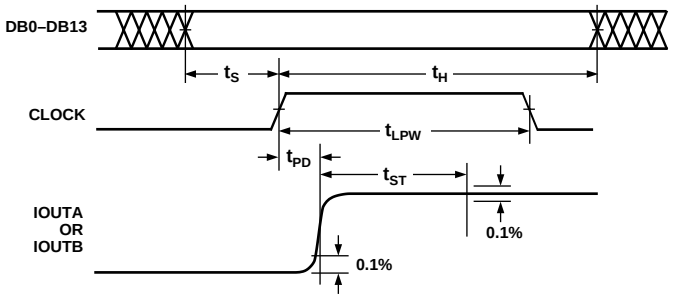


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–1.0	AVDD + 0.3	V
COMP1, COMP2	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
REFLO	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9764AR	–40 to +85°C	28-Lead SOIC_W	RW-28
AD9764ARRL	–40 to +85°C	28-Lead SOIC_W	RW-28
AD9764ARU	–40 to +85°C	28-Lead TSSOP	RU-28
AD9764ARURL7	–40 to +85°C	28-Lead TSSOP	RU-28
AD9764ARUZ	–40 to +85°C	28-Lead TSSOP	RU-28
AD9764ARUZRL7	–40 to +85°C	28-Lead TSSOP	RU-28
AD9764ARZ	–40 to +85°C	28-Lead SOIC_W	RW-28
AD9764ARZRL	–40 to +85°C	28-Lead SOIC_W	RW-28
AD9764-EBZ		Evaluation Board	

[1] RW = Small Outline IC, RU = TSSOP.
[2] Z = RoHS Compliant Part.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead 300 mil SOIC
θ_{JA} = 71.4° C/W
θ_{JC} = 23° C/W

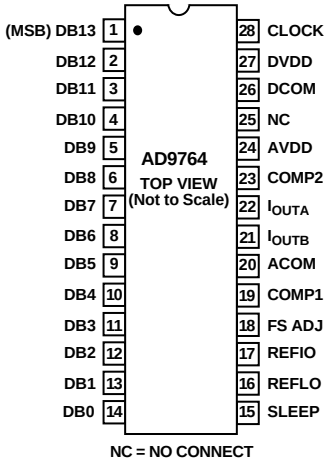
28-Lead TSSOP
θ_{JA} = 97.9° C/W
θ_{JC} = 14.0° C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9764 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DB13	Most Significant Data Bit (MSB).
2–13	DB12–DB1	Data Bits 1–12.
14	DB0	Least Significant Data Bit (LSB).
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit; it may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 μF capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
19	COMP1	Bandwidth/Noise Reduction Node. Add 0.1 μF to AVDD for optimum performance.
20	ACOM	Analog Common.
21	I_{OUTB}	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	I_{OUTA}	DAC Current Output. Full-scale current when all data bits are 1s.
23	COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 μF capacitor.
24	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
25	NC	No Internal Connection.
26	DCOM	Digital Common.
27	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
28	CLOCK	Clock Input. Data latched on positive edge of clock.

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied over a specified range.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the sum of the rms value of the first six harmonic components to the rms value of the measured output signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious-free dynamic range for an output containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

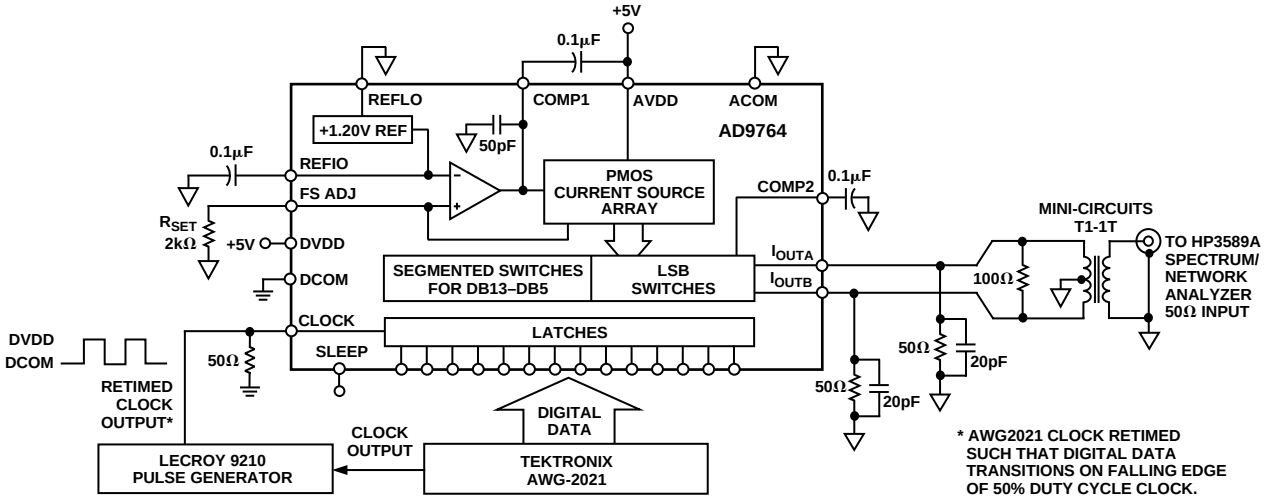


Figure 2. Basic AC Characterization Test Setup

Typical AC Characterization Curves

(AVDD = +5 V, DVDD = +3 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted)

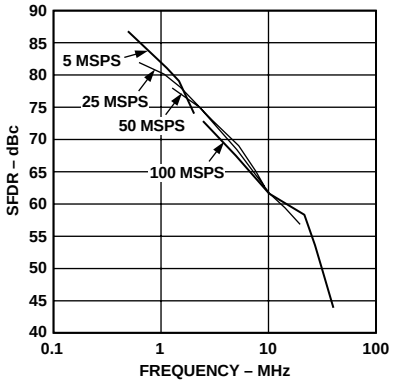


Figure 3. SFDR vs. f_{OUT} @ 0 dBFS

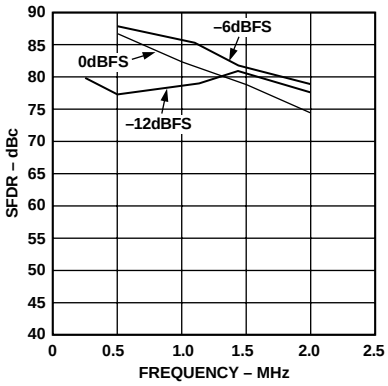


Figure 4. SFDR vs. f_{OUT} @ 5 MSPS

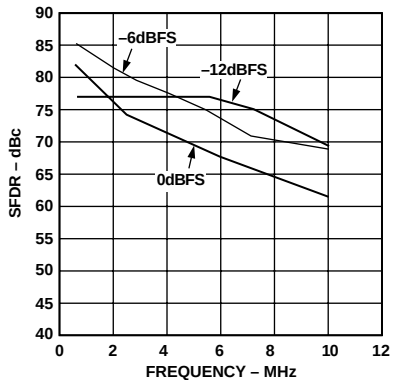


Figure 5. SFDR vs. f_{OUT} @ 25 MSPS

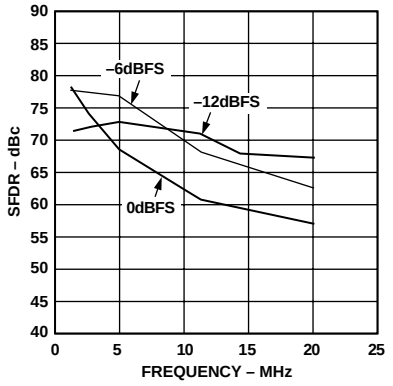


Figure 6. SFDR vs. f_{OUT} @ 50 MSPS

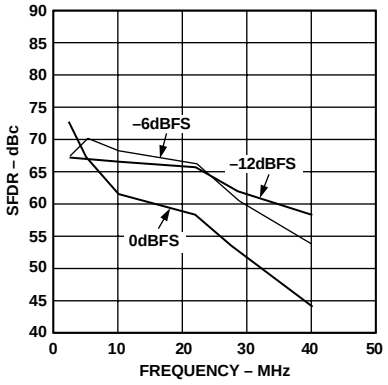


Figure 7. SFDR vs. f_{OUT} @100 MSPS

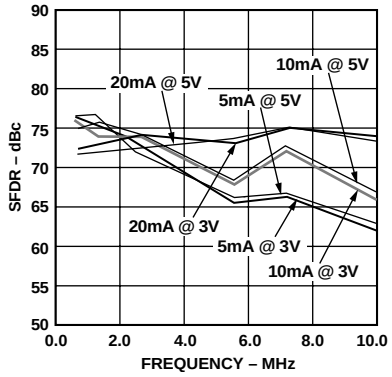


Figure 8. SFDR vs. f_{OUT} and I_{OUTFS} @ 25 MSPS and 0 dBFS

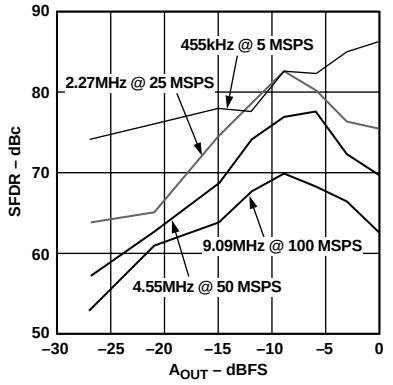


Figure 9. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

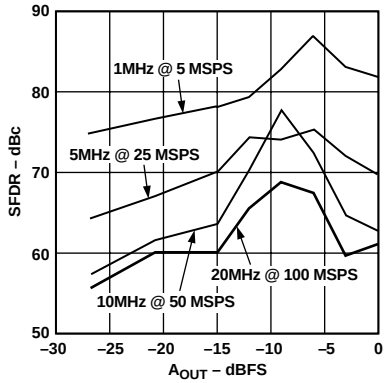


Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

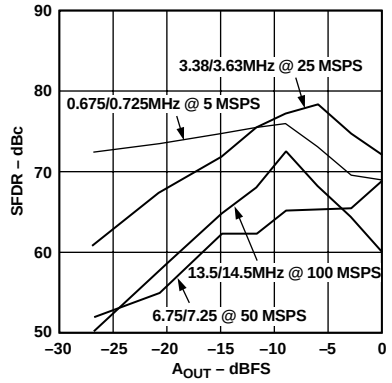


Figure 11. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/7$

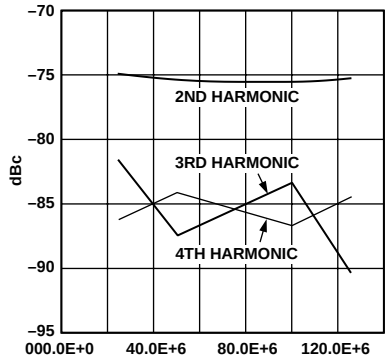


Figure 12. THD vs. f_{CLOCK} @ f_{OUT} = 2 MHz

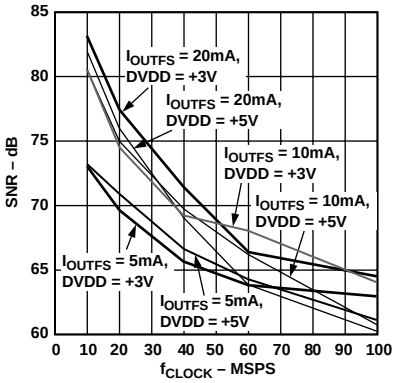


Figure 13. SNR vs. f_{CLOCK} @ f_{OUT} = 2.0 MHz

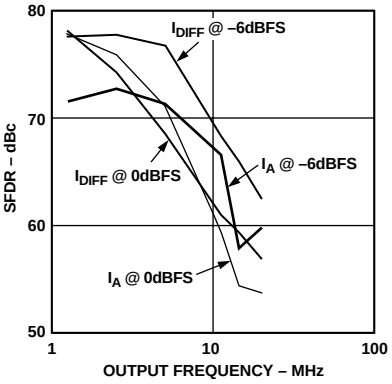


Figure 14. Differential vs. Single-Ended SFDR vs. f_{OUT} @ 50 MSPS

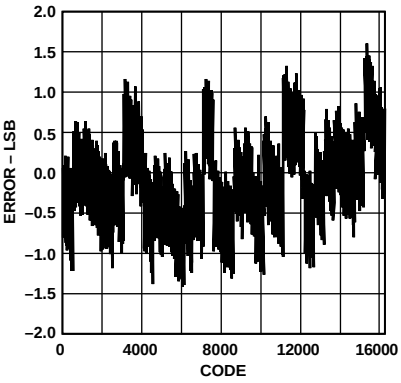


Figure 15. Typical INL

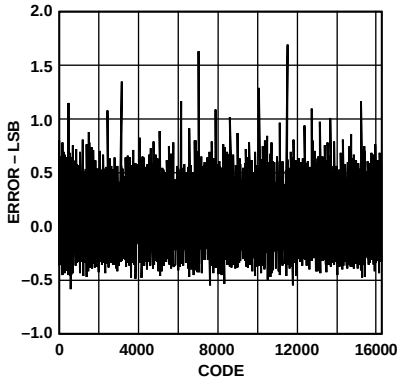


Figure 16. Typical DNL

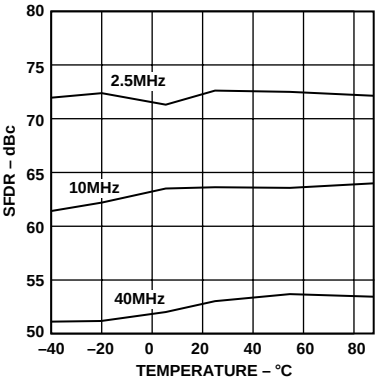


Figure 17. SFDR vs. Temperature @ 100 MSPS, 0 dBFS

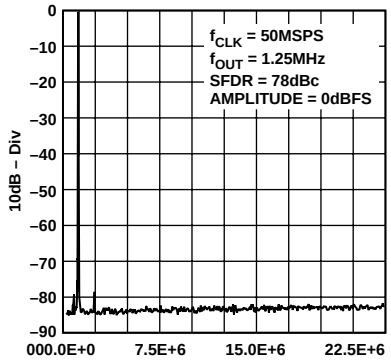


Figure 18. Single-Tone SFDR

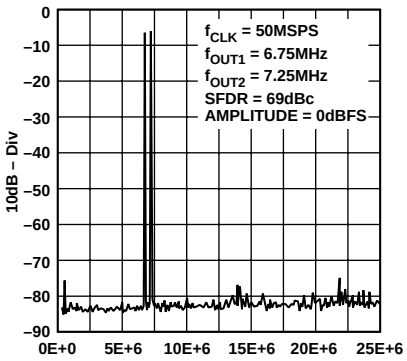


Figure 19. Dual-Tone SFDR

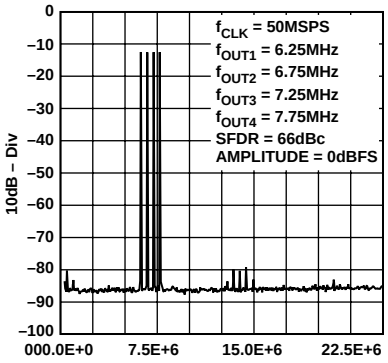


Figure 20. Four-Tone SFDR

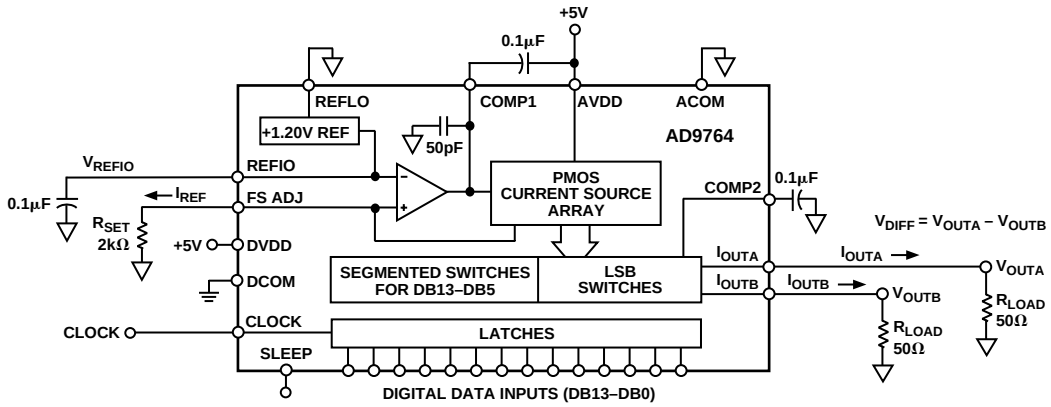


Figure 21. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Figure 21 shows a simplified block diagram of the AD9764. The AD9764 consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9764 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 2.7 volt to 5.5 volt range. The digital section, which is capable of operating up to a 125 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9764 provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE/16384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16383 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note that R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply:

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across I_{OUTA} and I_{OUTB} is:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 16383)/16384\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9764 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9764 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

REFERENCE OPERATION

The AD9764 contains an internal 1.20 V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output,* depending on whether the internal or external reference is selected. If REFLO is tied to ACOM, as shown in Figure 22, the internal reference is activated, and REFIO provides a 1.20 V output. In this case, the internal reference *must* be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. Also, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

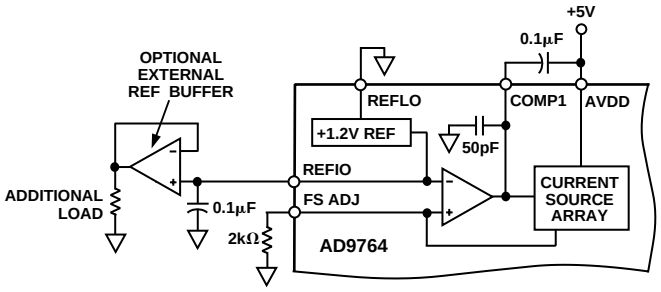


Figure 22. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 23. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

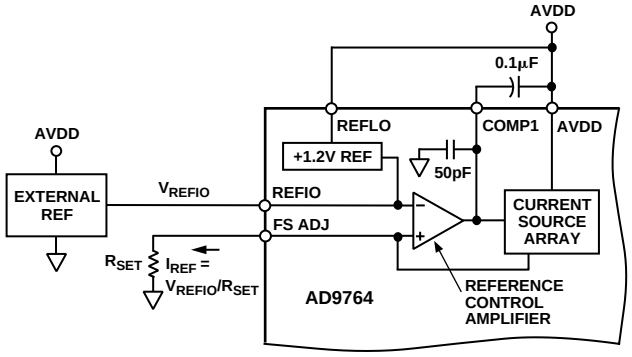


Figure 23. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9764 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 23, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting IREF between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9764, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 1.4 MHz and can be reduced by connecting an external capacitor between COMP1 and AVDD. The output of the control amplifier, COMP1, is internally compensated via a 50 pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. Figure 24 shows the relationship between the external capacitor and the small signal –3 dB bandwidth of the reference amplifier. Since the –3 dB bandwidth corresponds to the dominant pole, and hence the time constant, the settling time of the control amplifier to a stepped reference input response can be approximated.

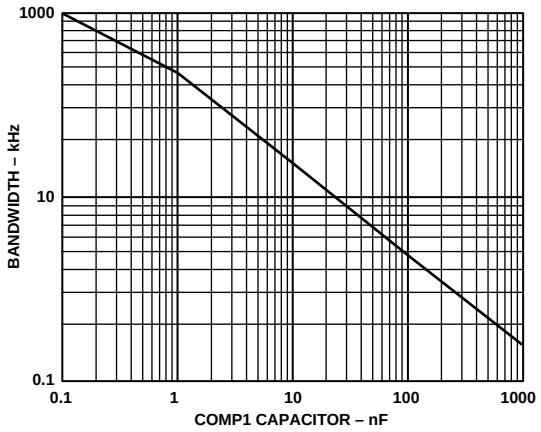


Figure 24. External COMP1 Capacitor vs. –3 dB Bandwidth

The optimum distortion performance for any reconstructed waveform is obtained with a 0.1 µF external capacitor installed. Thus, if I_{REF} is fixed for an application, a 0.1 µF ceramic chip capacitor is recommended. Also, since the control amplifier is optimized for low power operation, multiplying applications requiring large signal swings should consider using an external control amplifier to enhance the application's overall large signal multiplying bandwidth and/or distortion performance.

There are two methods in which I_{REF} can be varied for a fixed R_{SET}. The first method is suitable for a single-supply system in which the internal reference is disabled, and the common-mode voltage of REFIO is varied over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1 MΩ, a simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 25 using the AD7524 and an external 1.2 V reference, the AD1580.

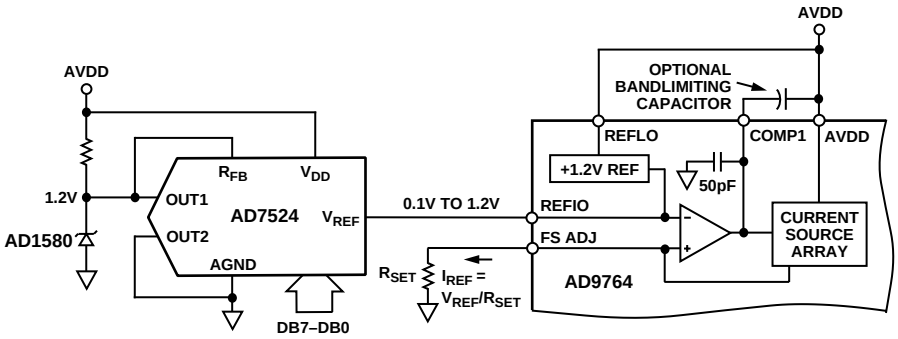


Figure 25. Single-Supply Gain Control Circuit

The second method may be used in a dual-supply system in which the common-mode voltage of REFIO is fixed, and I_{REF} is varied by an external voltage, V_{GC}, applied to R_{SET} via an amplifier. An example of this method is shown in Figure 26 in which the internal reference is used to set the common-mode voltage of the control amplifier to 1.20 V. The external voltage, V_{GC}, is referenced to ACOM and should not exceed 1.2 V. The value of R_{SET} is such that I_{REFMAX} and I_{REFMIN} do not exceed 62.5 μA and 625 μA, respectively. The associated equations in Figure 26 can be used to determine the value of R_{SET}.

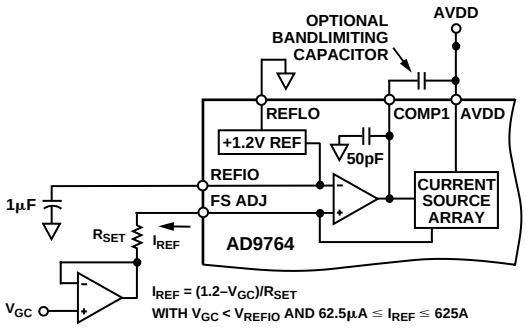


Figure 26. Dual-Supply Gain Control Circuit

In some applications, the user may elect to use an external control amplifier to enhance the multiplying bandwidth, distortion performance and/or settling time. External amplifiers capable of driving a 50 pF load such as the AD817 are suitable for this purpose. It is configured in such a way that it is in parallel with the weaker internal reference amplifier as shown in Figure 27. In this case, the external amplifier simply overdrives the weaker reference control amplifier. Also, since the internal control amplifier has a limited current output, it will sustain no damage if overdriven.

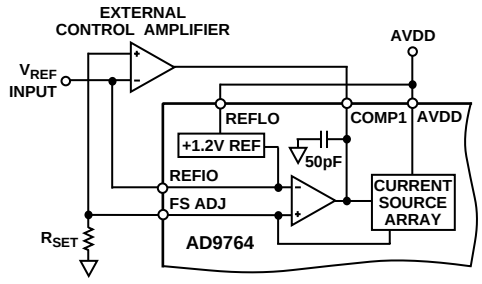


Figure 27. Configuring an External Reference Control Amplifier

ANALOG OUTPUTS

The AD9764 produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be configured for single-end or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 28 shows the equivalent analog output circuit of the AD9764 consisting of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches and is typically 100 kΩ in parallel with 5 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, AVDD, and full-scale current, I_{OUTFS}. Although the output impedance's signal dependency can be a source of dc nonlinearity and ac linearity (i.e., distortion), its effects can be limited if certain precautions are noted.

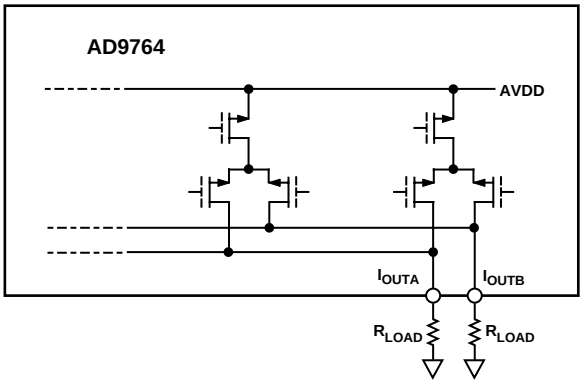


Figure 28. Equivalent Analog Output Circuit

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9764. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal

1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. Operation beyond the positive compliance range will induce clipping of the output signal which severely degrades the AD9764's linearity and distortion performance.

For applications requiring the optimum dc linearity, I_{OUTA} and/or I_{OUTB} should be maintained at a virtual ground via an I-V op amp configuration. Maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground keeps the output impedance of the AD9764 fixed, significantly reducing its effect on linearity. However, it does not necessarily lead to the optimum distortion performance due to limitations of the I-V op amp. Note that the INL/DNL specifications for the AD9764 are measured in this manner using I_{OUTA}. In addition, these dc linearity specifications remain virtually unaffected over the specified power supply range of 2.7 V to 5.5 V.

Operating the AD9764 with reduced voltage output swings at I_{OUTA} and I_{OUTB} in a differential or single-ended output configuration reduces the signal dependency of its output impedance thus enhancing distortion performance. Although the voltage compliance range of I_{OUTA} and I_{OUTB} extends from –1.0 V to +1.25 V, optimum distortion performance is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed approximately 0.5 V. A properly selected transformer with a grounded center-tap will allow the AD9764 to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at I_{OUTA} and I_{OUTB}. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to Applying the AD9764 section for examples of various output configurations.

The most significant improvement in the AD9764's distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed waveform's frequency content increases and/or its amplitude decreases. This is evident in Figure 14, which compares the differential vs. single-ended performance of the AD9764 at 50 MSPS for 0.0 and –6.0 dBFS single tone waveforms over frequency.

The distortion and noise performance of the AD9764 is also slightly dependent on the analog and digital supply as well as the full-scale current setting, I_{OUTFS}. Operating the analog supply at 5.0 V ensures maximum headroom for its internal PMOS current sources and differential switches leading to improved distortion performance as shown in Figure 8. Although I_{OUTFS} can be set between 2 mA and 20 mA, selecting an I_{OUTFS} of 20 mA will provide the best distortion and noise performance also shown in Figure 8. The noise performance of the AD9764 is affected by the digital supply (DVDD), output frequency, and increases with increasing clock rate as shown in Figure 13. Operating the AD9764 with low voltage logic levels between 3 V and 3.3 V will slightly reduce the amount of on-chip digital noise.

In summary, the AD9764 achieves the optimum distortion and noise performance under the following conditions:

(1) Differential Operation.

(2) Positive voltage swing at I_{OUTA} and I_{OUTB} limited to +0.5 V.

(3) I_{OUTFS} set to 20 mA.

(4) Analog Supply (AVDD) set at 5.0 V.

(5) Digital Supply (DVDD) set at 3.0 V to 3.3 V with appropriate logic levels.

Note that the ac performance of the AD9764 is characterized under the above mentioned operating conditions.

DIGITAL INPUTS

The AD9764's digital input consists of 14 data input pins and a clock input pin. The 14-bit parallel data inputs follow standard positive binary coding where DB13 is the most significant bit (MSB), and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock as shown in Figure 1 and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

The digital inputs are CMOS-compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (DVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9764 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers $V_{OH(MAX)}$. A DVDD of 3 V to 3.3 V will typically ensure proper compatibility with most TTL logic families. Figure 29 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, thus ensuring that the AD9764 remains enabled if this input is left disconnected.

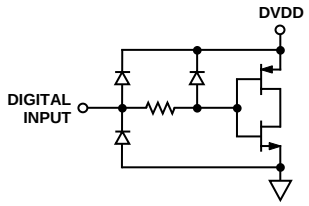


Figure 29. Equivalent Digital Input

Since the AD9764 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9764 with reduced logic swings and a corresponding digital supply (DVDD) will result in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9764 as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9764 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs.

The external clock driver circuitry should provide the AD9764 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note, that the clock input could also be driven via a sine wave, which is centered around the digital threshold (i.e., DVDD/2) and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and, subsequently, cut into the required data setup and hold times.

SLEEP MODE OPERATION

The AD9764 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the AD9764 remains enabled if this input is left disconnected. The SLEEP input with active pull-down requires <40 μA of drive current.

The power-up and power-down characteristics of the AD9764 are dependent upon the value of the compensation capacitor connected to COMP1. With a nominal value of 0.1 μF, the AD9764 takes less than 5 μs to power down and approximately 3.25 ms to power back up. Note, the SLEEP MODE should not be used when the external control amplifier is used as shown in Figure 27.

POWER DISSIPATION

The power dissipation, P_D, of the AD9764 is dependent on several factors, including: (1) AVDD and DVDD, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; and (4) the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 30, and is insensitive to f_{CLOCK}.

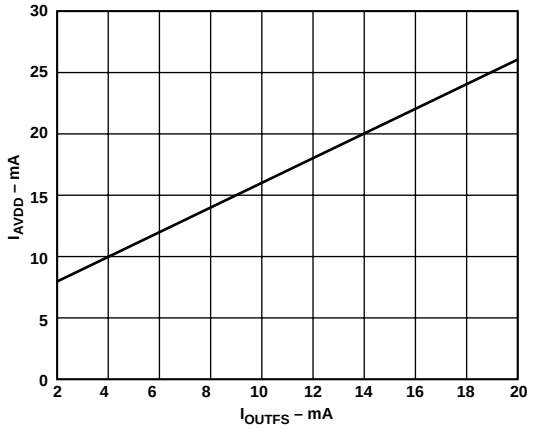


Figure 30. I_{AVDD} vs. I_{OUTFS}

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 31 and 32 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note, how I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

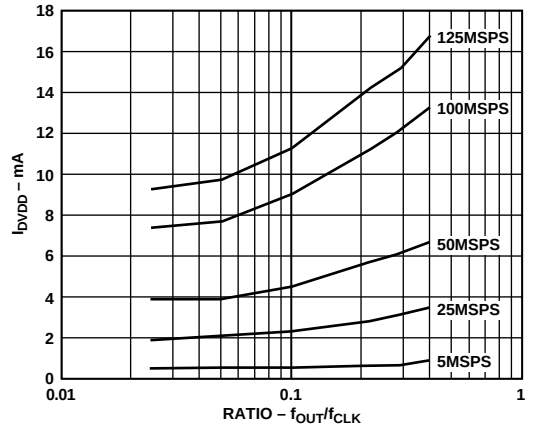


Figure 31. I_{DVDD} vs. Ratio @ DVDD = 5 V

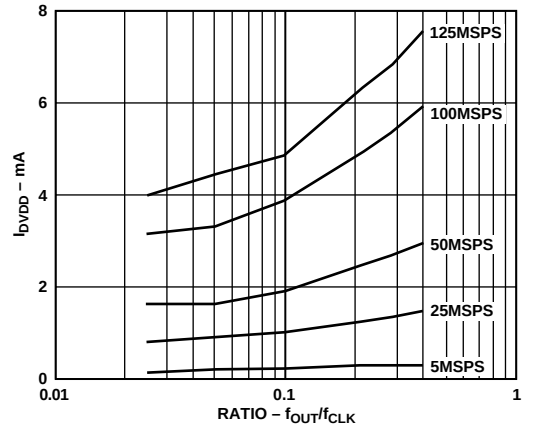


Figure 32. I_{DVDD} vs. Ratio @ DVDD = 3 V

APPLYING THE AD9764

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9764. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note, I_{OUTA} provides slightly better performance than I_{OUTB}.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 33. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

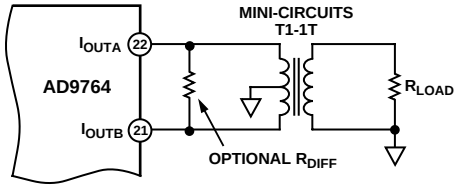


Figure 33. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9764. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 34. The AD9764 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's high slewing output from overloading the op amp's input.

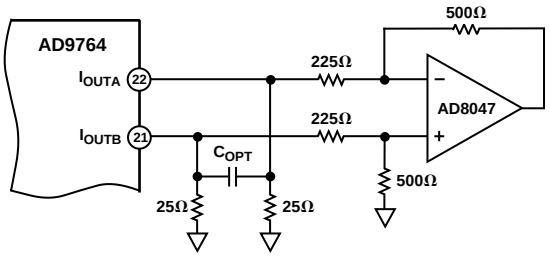


Figure 34. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9764 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 35 provides the necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the AD9764 and the op amp, is also used to level-shift the differential output of the AD9764 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

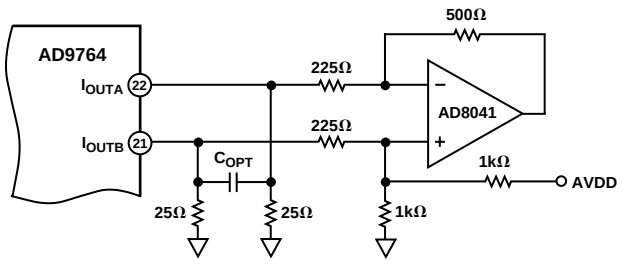


Figure 35. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 36 shows the AD9764 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of

I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

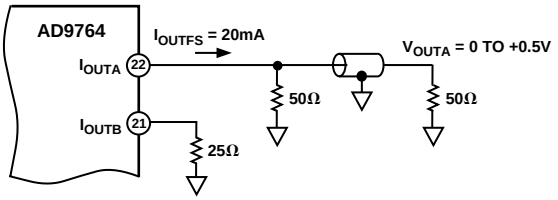


Figure 36. 0 V to +0.5 V Unbuffered Voltage Output

SINGLE-ENDED BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 37 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9764 output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

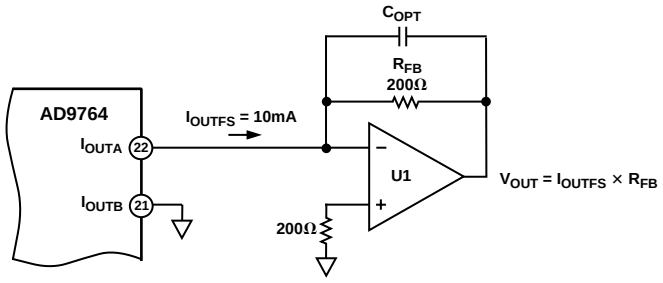


Figure 37. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing and supply bypassing and grounding. Figures 42–47 illustrate the recommended printed circuit board ground, power and signal plane layouts that are implemented on the AD9764 evaluation board.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9764 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically as possible.

For those applications requiring a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 38. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

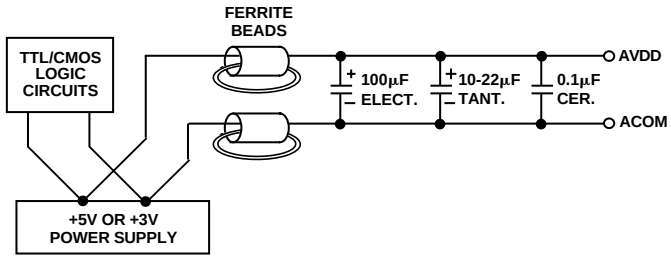


Figure 38. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtain optimum results from the AD9764. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistors should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

MULTITONE PERFORMANCE CONSIDERATIONS AND CHARACTERIZATION

The frequency domain performance of high speed DACs has traditionally been characterized by analyzing the spectral output of a reconstructed full-scale (i.e., 0 dBFS), single-tone sine wave at a particular output frequency and update rate. Although this characterization data is useful, it is often insufficient to reflect a DAC's performance for a reconstructed multitone or spread-spectrum waveform. In fact, evaluating a DAC's spectral performance using a full-scale, single tone at the highest specified frequency (i.e., f_H) of a bandlimited waveform is typically indicative of a DAC's "worst-case" performance for that given waveform. In the time domain, this full-scale sine wave represents the lowest peak-to-rms ratio or crest factor (i.e., V_{PEAK}/V rms) that this bandlimited signal will encounter.

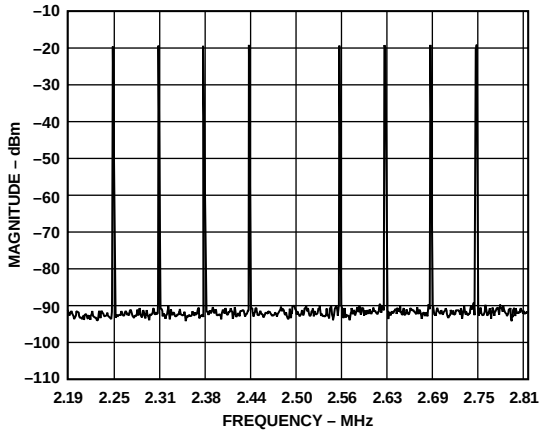


Figure 39a. Multitone Spectral Plot

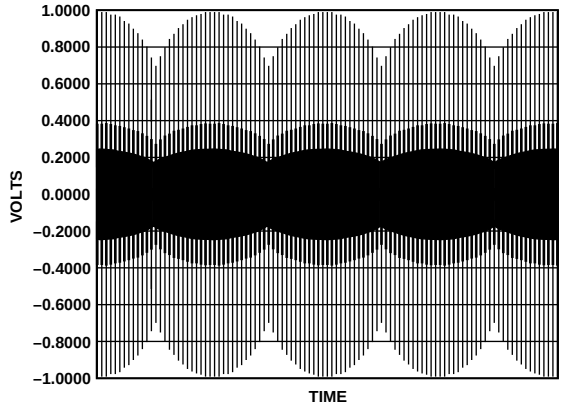


Figure 39b. Time Domain "Snapshot" of the Multitone Waveform

However, the inherent nature of a multitone, spread spectrum, or QAM waveform, in which the spectral energy of the waveform is spread over a designated bandwidth, will result in a higher peak-to-rms ratio when compared to the case of a simple sine wave. As the reconstructed waveform's peak-to-average ratio increases, an increasing amount of the signal energy is concentrated around the DAC's midscale value. Figure 39a is just one example of a bandlimited multitone vector (i.e., eight tones) centered around one-half the Nyquist bandwidth (i.e., $f_{CLOCK}/4$). This particular multitone vector, has a peak-to-rms ratio of 13.5 dB compared to a sine waves peak-to-rms ratio of 3 dB. A "snapshot" of this reconstructed multitone vector in the time domain as shown in Figure 39b reveals the higher signal content around the midscale value. As a result, a DAC's "small-scale" dynamic and static linearity becomes increasingly critical in obtaining low intermodulation distortion and maintaining sufficient carrier-to-noise ratios for a given modulation scheme.

A DAC's small-scale linearity performance is also an important consideration in applications where additive dynamic range is required for gain control purposes or "predistortion" signal conditioning. For instance, a DAC with sufficient dynamic range can be used to provide additional gain control of its reconstructed signal. In fact, the gain can be controlled in 6 dB increments by simply performing a shift left or right on the DAC's digital input word. Other applications may intentionally predistort a DAC's digital input signal to compensate for nonlinearities associated with the subsequent analog components in the signal chain. For example, the signal compression associated with a power amplifier can be compensated for by predistorting the DAC's digital input with the inverse nonlinear transfer function of the power amplifier. In either case, the DAC's performance at reduced signal levels should be carefully evaluated.

A full-scale single tone will induce all of the dynamic and static nonlinearities present in a DAC that contribute to its distortion and hence SFDR performance. Referring to Figure 3, as the frequency of this reconstructed full-scale, single-tone waveform increases, the dynamic nonlinearities of any DAC (i.e., AD9764) tend to dominate thus contributing to the rolloff in its SFDR performance. However, unlike most DACs, which employ an R-2R ladder for the lower bit current segmentation, the AD9764 (as well as other TxDAC members) exhibits an improvement in distortion performance as the amplitude of a single tone is reduced from its full-scale level. This improvement in distortion performance at reduced signal levels is evident if one compares the SFDR performance vs. frequency at different amplitudes (i.e., 0 dBFS, –6 dBFS and –12 dBFS) and sample rates as shown in Figures 4 through 7. Maintaining decent "small-scale" linearity across the full span of a DAC transfer function is also critical in maintaining excellent multitone performance.

Although characterizing a DAC's multitone performance tends to be application-specific, much insight into the potential performance of a DAC can also be gained by evaluating the DAC's swept power (i.e., amplitude) performance for single, dual and multitone test vectors at different clock rates and carrier frequencies. The DAC is evaluated at different clock rates when reconstructing a specific waveform whose amplitude is decreased in 3 dB increments from full-scale (i.e., 0 dBFS). For each specific waveform, a graph showing the SFDR (over Nyquist) performance vs. amplitude can be generated at the different tested clock rates as shown in Figures 9–11. Note that the carrier(s)-to-clock ratio remains constant in each figure. In each case, an improvement in SFDR performance is seen as the amplitude is reduced from 0 dBFS to approximately –9.0 dBFS.

A multitone test vector may consist of several equal amplitude, spaced carriers each representative of a channel within a defined bandwidth as shown in Figure 39a. In many cases, one or more tones are removed so the intermodulation distortion performance

of the DAC can be evaluated. Nonlinearities associated with the DAC will create spurious tones of which some may fall back into the "empty" channel thus limiting a channel's carrier-to-noise ratio. Other spurious components falling outside the band of interest may also be important, depending on the system's spectral mask and filtering requirements.

This particular test vector was centered around one-half the Nyquist bandwidth (i.e., $f_{CLOCK}/4$) with a passband of $f_{CLOCK}/16$. Centering the tones at a much lower region (i.e., $f_{CLOCK}/10$) would lead to an improvement in performance while centering the tones at a higher region (i.e., $f_{CLOCK}/2.5$) would result in a degradation in performance. Figure 40a shows the SFDR vs. amplitude at different sample rates up to the Nyquist frequency while Figure 40b shows the SFDR vs. amplitude within the passband of the test vector. In assessing a DAC's multitone performance, it is also recommended that several units be tested under exactly the same conditions to determine any performance variability.

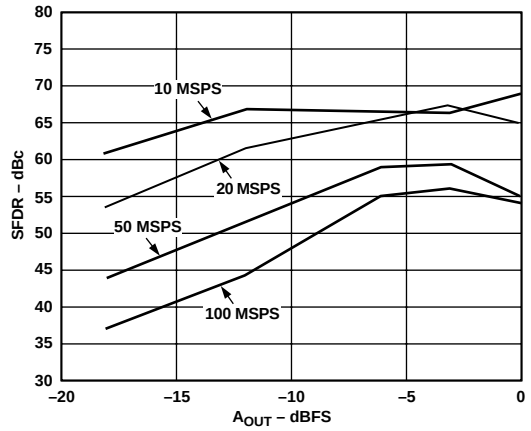


Figure 40a. Multitone SFDR vs. A_{OUT} (Up to Nyquist)

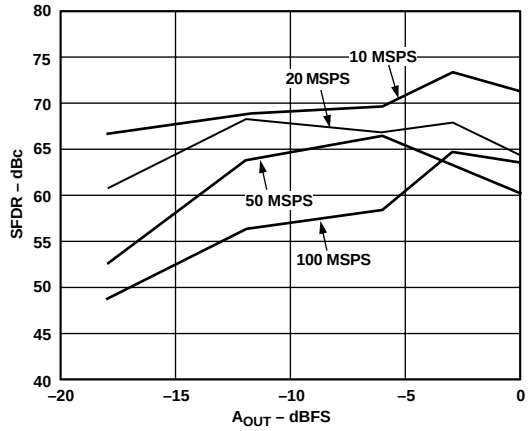


Figure 40b. Multitone SFDR vs. A_{OUT} (Within Multitone Passband)

AD9764 EVALUATION BOARD

General Description

The AD9764-EB is an evaluation board for the AD9764 14-bit DAC converter. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to easily and effectively evaluate the AD9764 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9764 in various configurations. Possible output configurations include transformer coupled, resistor terminated, inverting/noninverting and differential amplifier outputs. The digital inputs are designed to be driven directly from various word generators with the onboard option to add a resistor network for proper load termination. Provisions are also made to operate the AD9764 with either the internal or external reference or to exercise the power-down feature.

Refer to the application note AN-420, *Using the AD9760/AD9764/AD9764-EB Evaluation Board* for a thorough description and operating instructions for the AD9764 evaluation board.

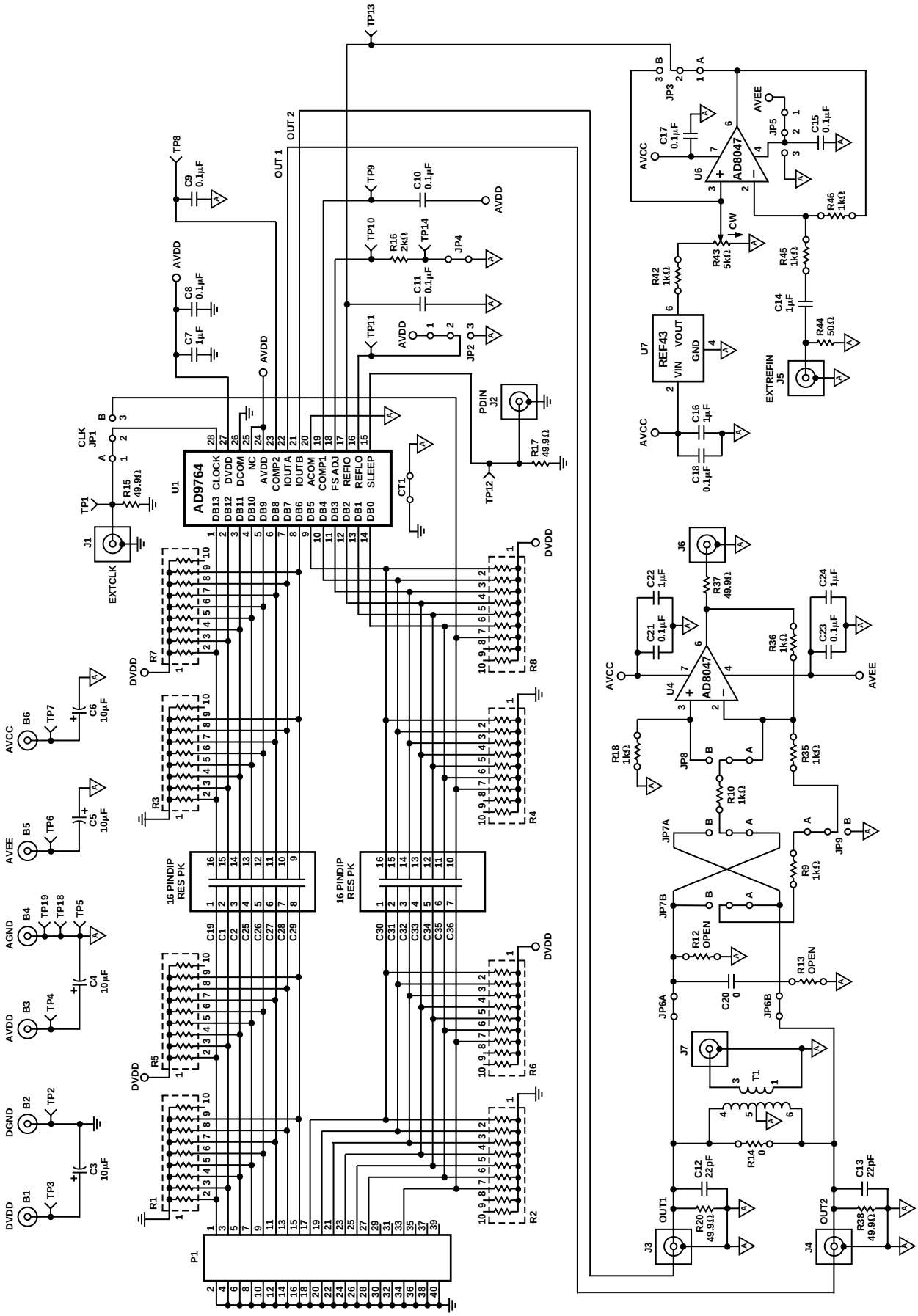


Figure 41. Evaluation Board Schematic

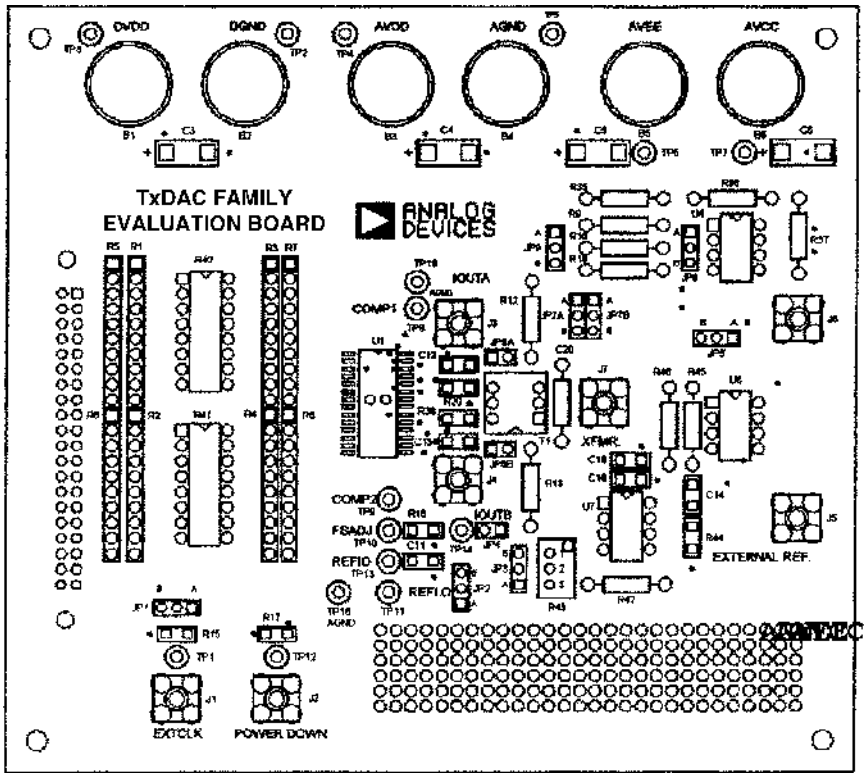


Figure 42. Silkscreen Layer—Top

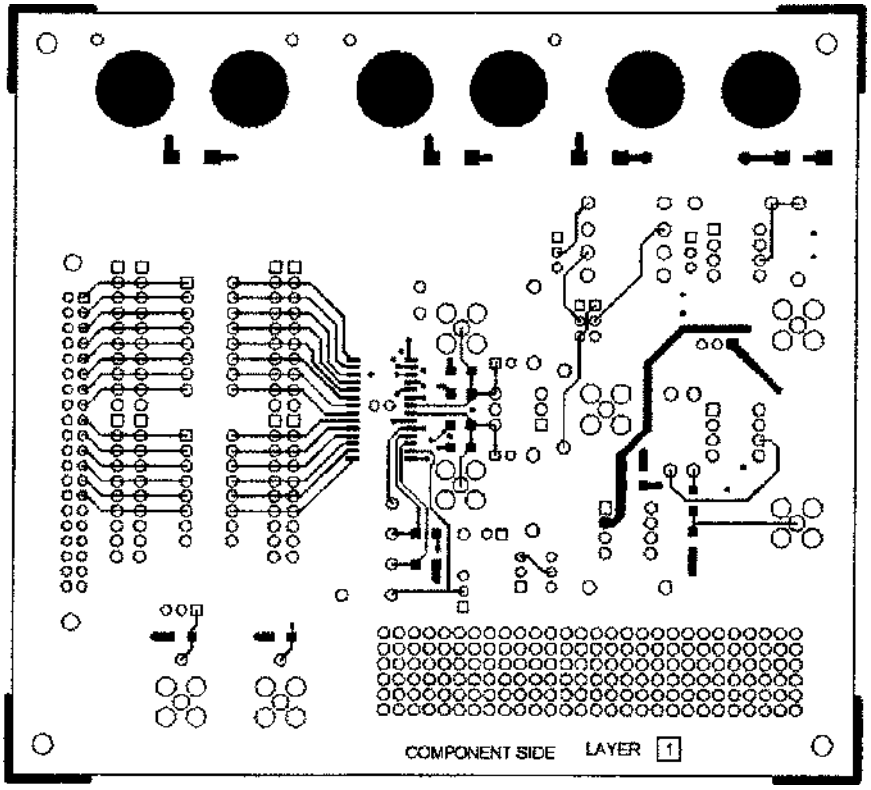


Figure 43. Component Side PCB Layout (Layer 1)

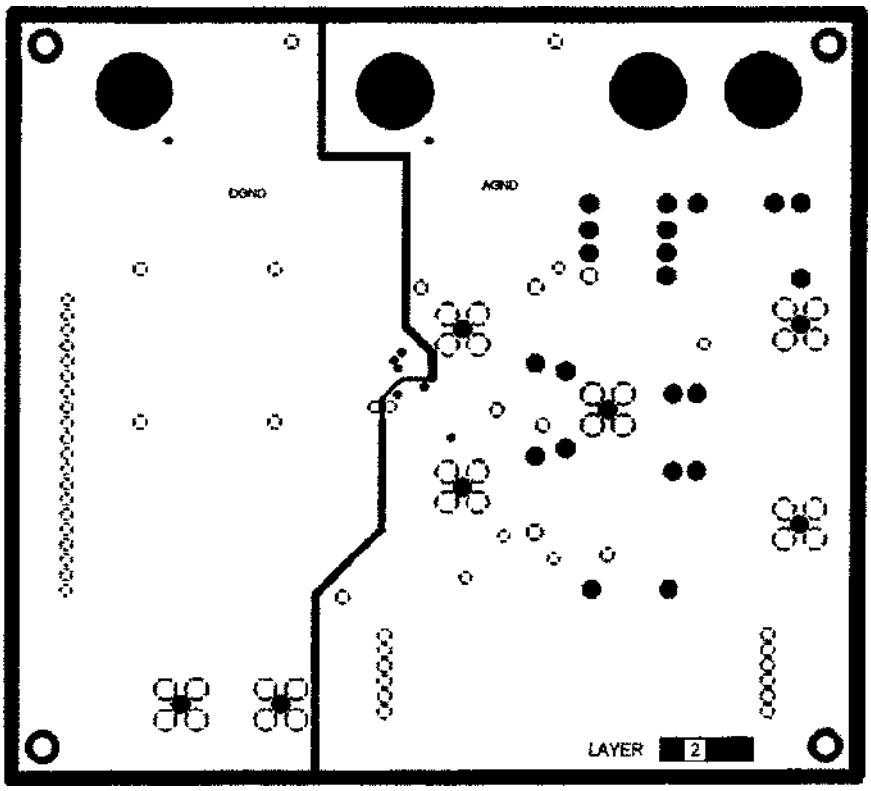


Figure 44. Ground Plane PCB Layout (Layer 2)

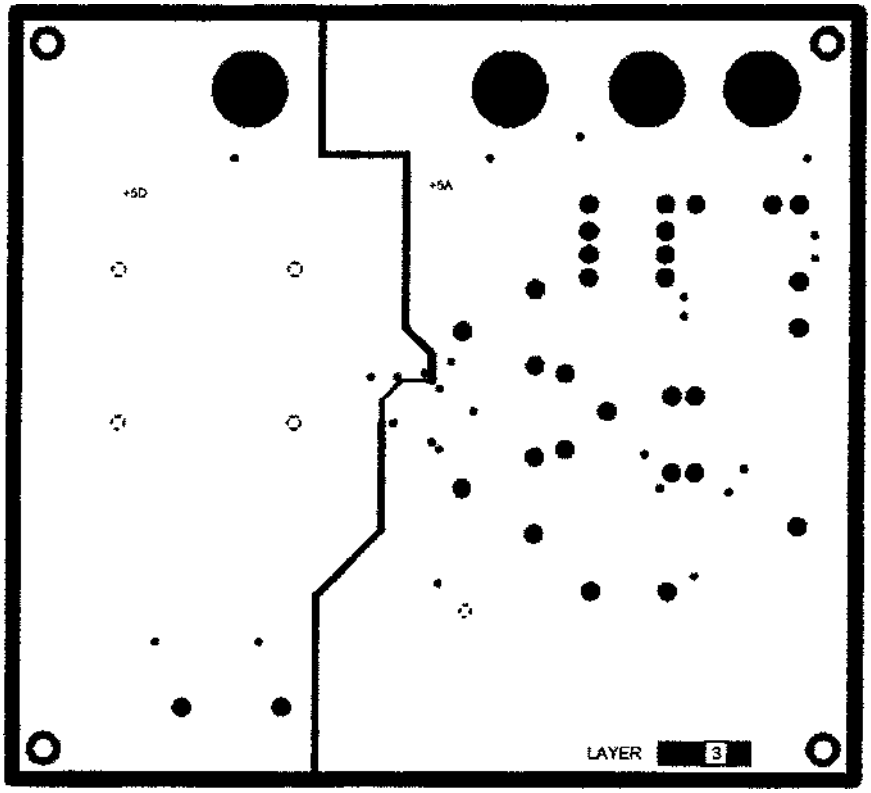


Figure 45. Power Plane PCB Layout (Layer 3)

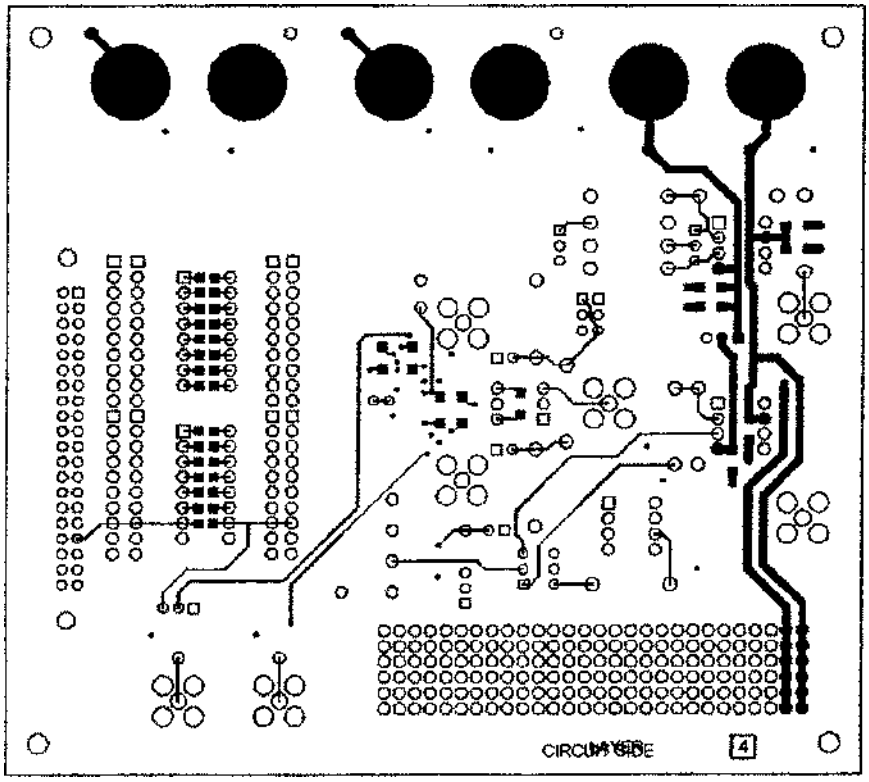


Figure 46. Solder Side PCB Layout (Layer 4)

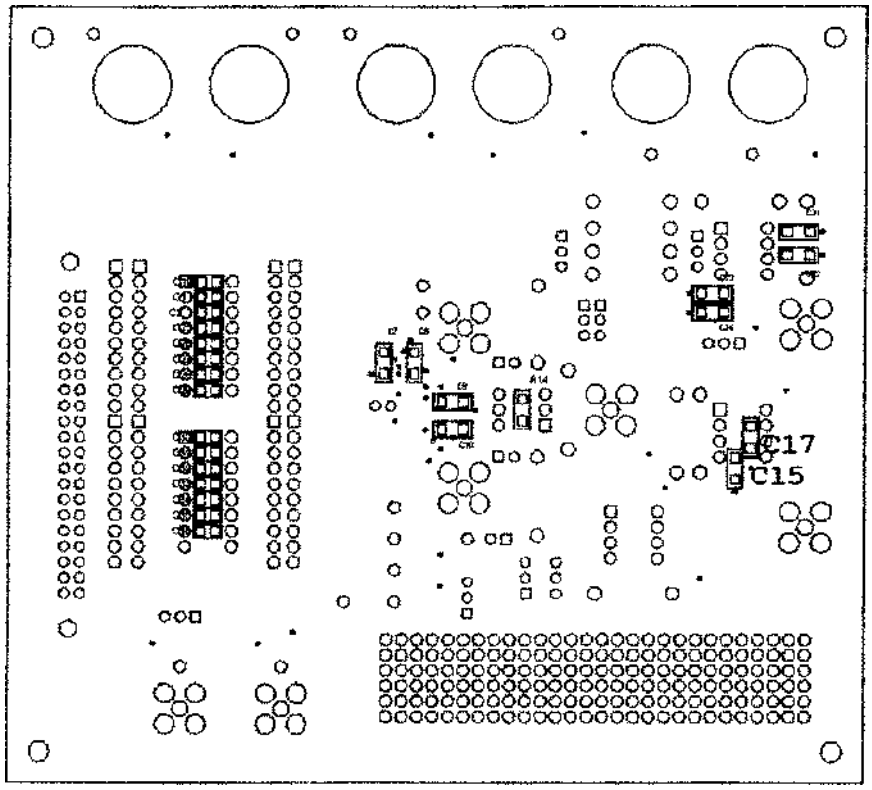
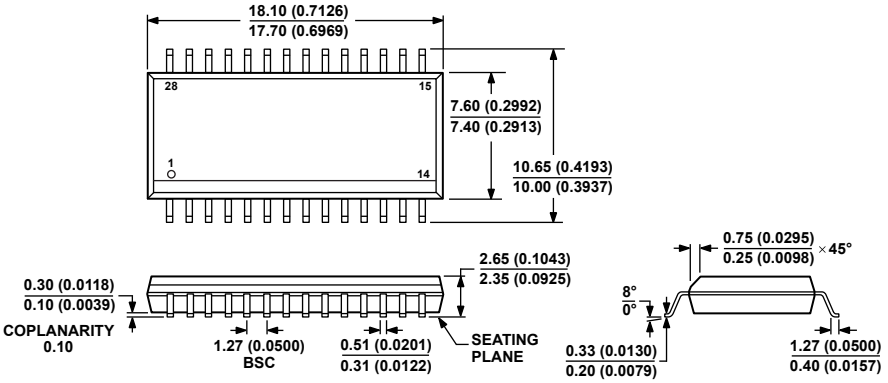


Figure 47. Silkscreen Layer—Bottom

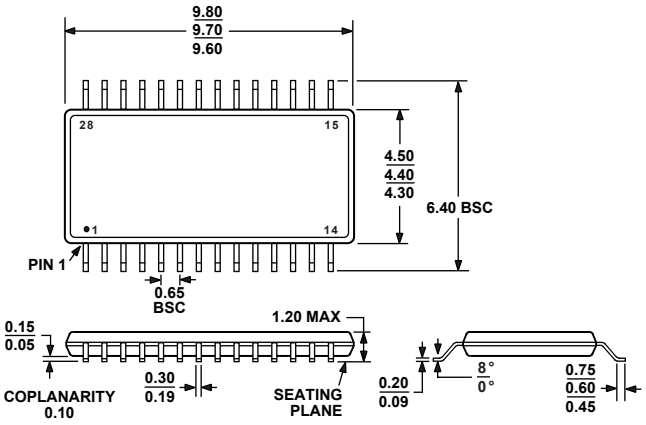
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Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AE

28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

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